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12EC025

M.Tech. Degree Examination, June/July 2013

Design of Analog and Mixed Mode VLSI Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Derive and explain I/V characteristics of MOSFET from fundamental concept. **(12 Marks)**

b. Plot the variation of gate to source and gate to drain capacitance as function of gate to source voltage in different regions of operations of a MOSFET. Give explanation for each region. **(08 Marks)**

2 a. Derive an expression for voltage gain and output resistance of common source stage with source degeneration $\lambda \neq 0$ and $r \neq 0$. **(15 Marks)**

b. Calculate the voltage gain of the circuit shown in Fig.Q2(b). **(05 Marks)**

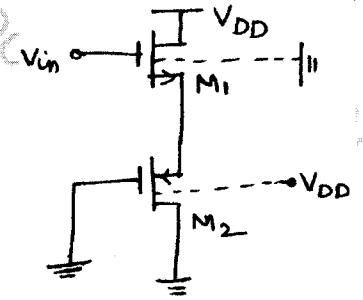

Fig.Q2(b)

3 a. Calculate the voltage gain of the circuit in Fig.Q3(a) if $\lambda \neq 0$ and $r \neq 0$.

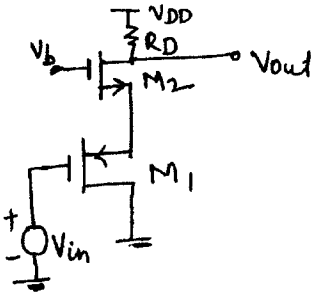

Fig.Q3(a) **(10 Marks)**

b. Give the circuit of folded cascade stage with PMOS input transistor and obtain its large signal characteristics V_{out} versus V_{in}. **(10 Marks)**

4 a. Calculate the input resistance of the circuit shown in Fig.Q4(a).

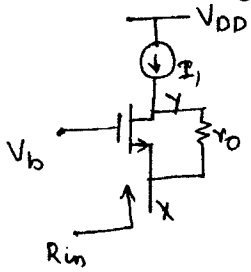

Fig.Q4(a) **(06 Marks)**

4 b. Obtain the high frequency model of a common source stage. Obtain its transfer function and discuss its frequency response. **(14 Marks)**

5 a. For the circuit shown in Fig.Q5(a), find:
i) What is the required input CM for which R_{ss} sustains 0.5V?
ii) Calculate R_D for a differential gain of 5.
iii) What happens at the output, if the input CM level is 50 mV higher than the value calculated in (i)?

Assume: $\left(\frac{W}{L}\right)_{1,2} = \frac{25}{0.5}$, $\mu_{nCox} = 50\mu A/V^2$, $V_{Th} = 0.6$ V, $\lambda = r = 0$, $V_{DD} = 3$V,

Tail current = 1 mA, $R_{D1} = R_{D2} = R_D$

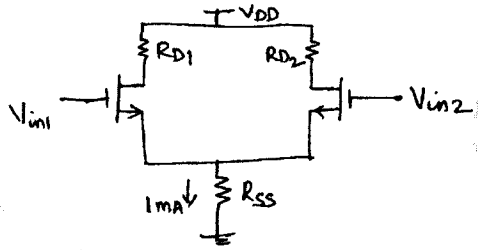

Fig.Q5(a) **(10 Marks)**

b. Explain the operation of Gilbert cell. **(10 Marks)**

6 a. What is VCO? Explain VCO. **(04 Marks)**
b. Explain important performance parameters of VCO's. **(08 Marks)**
c. A VCO sensor a small sinusoidal control voltage $V_{cont} = V_m \cos(w_m t)$. Determine the output waveform and its spectrum. **(08 Marks)**

7 a. Explain the operation of current steering DAC architecture with neat diagrams and equations. **(10 Marks)**
b. Explain the operation of pipeline ADC architecture with neat diagrams and example. **(10 Marks)**

8 Write technical notes on the following:
a. PLL as a frequency synthesizer. **(10 Marks)**
b. Resistor string DAC using binary switch array. **(10 Marks)**

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